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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Ted A. Loxley

Serial No.: 09/490,162

Group No.: 2812

Filed: January 22, 2000

Examiner: V. Simkovic

For: PROCESS AND APPARATUS FOR CLEANING SILICON WAFERS

Box AF

Assistant Commissioner for Patents

Washington, D.C. 20231

AMENDMENT TRANSMITTAL

1. Transmitted herewith is an amendment for this application.

STATUS

2. Applicant is
 - ☒ a small entity — verified statement:
 - ☐ attached.
 - ☒ already filed.
 - ☐ other than a small entity.

CERTIFICATE OF MAILING (37 CFR 1.8a)

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being deposited with the United State Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to the: Commissioner of Patents and Trademarks, Washington, D.C. 20231.

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TC 2800 MAIL ROOM
#9/C (A/E)
1/25/02
V. Varnal

Box AF
Assistant Commissioner for Patents
Washington, D.C. 20231

AMENDMENT AFTER FINAL REJECTION

Sir:

In response to the final Office action of October 19, 2001, please amend the above-identified application as follows:

Cancel claims 19 and 20 and rewrite as follows:

-- 19. (Amended) A process according to claim 18 wherein the front face of the process wafer is subjected to wet CMP polishing with colloidal silica or alumina particles having an average particle size of from 0.01 to 0.03 microns and is thereafter subjected to chemical cleaning and DI rinsing operations while said front face is negatively charged to a voltage sufficient to cause substantially complete removal of sub 0.05-micron killer particles bonded to the wafer surface.

20. (Amended) A process according to claim 1 for fabrication of microchips having a minimum line width or circuit image size less than 0.15 microns wherein the front face of each

wafer is subjected to the wet CMP polishing with colloidal silica or alumina particles and is thereafter subjected to a wet cleaning operation for 0.5 to 5 minutes while said front face is negatively charged to a limited voltage of 10 to 40 volts or more sufficient to cause substantially complete removal of sub 0.05-micron killer particles, the voltage and rate of charge of the wafer surface being applied or controlled during said wet cleaning operation in such manner as to minimize or limit damage or alteration of the delicate microcircuitry. --

Cancel claims 23, 29 and 30 without prejudice.

Add the following claim:

-- 32. (New) A process according to claim 19 wherein the front face of the wafer is provided with a limited electric charge of at least 10 volts during the wet cleaning operations. --

Cancel claim 14 and rewrite in independent form as follows:

-- 33. (New) In the fabrication of microelectronic devices on silicon semiconductor wafers where delicate microcircuits are formed on the front face of a flat silicon wafer having a diameter of at least 200 mm by more than 200 steps including many layering, patterning and doping operations and at least 30 wet processing steps, the improvement wherein each semiconductor wafer is electrically charged to a voltage of from 2 to 60 volts during wet processing operations to provide an effective field intensity sufficient to dislodge and repel harmful sub 0.05-micron particles and wherein the front face of one wafer containing the delicate microcircuits is subjected to a